COPLANAR WAVEGUIDE BASED, DIELECTRIC COATED FLIP CHIP MONOLITHIC MICROWAVE INTEGRATED CIRCUIT, A PARADIGM SHIFT IN MMIC TECHNOLOGY*

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ABSTRACT

The status of a coplanar waveguide based, novel dielectric coated, mechanically rugged, flip-chip, monolithic microwave integrated circuit (MMIC) technology will be described. This technology is ideal for low-cost, multi-chip transmit/receive (T/R) module applications. Equivalent circuit and thermal models, and the fabrication procedure of flip-chip MMICs featuring T-shaped plated silver thermal bumps will be presented along with test results obtained on components designed using these circuit element models.

* The work is partially supported by a cooperative grant from the Advanced Technology Program (ATP) Office of the National Institute of Standards and Technology (NIST).

SUMMARY

Rapid expansion of microwave systems in commercial applications in the emerging wireless communication and remote sensing/control system areas requires affordable, compact size, light weight, reliable solid state integrated microwave transmit/receive (T/R) modules. Current microwave modules fabricated using microstrip based hybrid/monolithic integrated circuitry are incompatible with low cost, high volume, robotics manufacturing techniques because of the fragile nature of existing gallium arsenide monolithic microwave integrated circuits (MMICs). A novel flip-chip approach to microwave T/R module using rugged, passivated MMIC chips with coplanar waveguide circuitry, on-chip multi-layer metal interconnects, off-chip plated metal electrical/thermal paths offers major advantages over conventional MMICs (Table 1).

In place of wire bonding off-chip electrical interconnects, the MMIC chips are flipped over (Fig. 1), and the electrical connects are made through plated electrodes (bumps) directly from the surface of the chips to the surface of the module substrate, using a solder reflow process. Besides the advantage of eliminating bondwires, the flip chip process allows electrical connection anywhere on a chip surface, not only at the periphery. The surface tension of the melted solder also provide precision self-alignment of a MMIC to the printed solder pattern on the substrate, leading to a single-step, solder reflow, multi-chip module assembly process.

Plated silver thermal bumps fabricated on top of the active circuit elements (i. e. plated gold bridges connecting the source electrodes of a multi-cell field effect transistor) can provide low resistance thermal paths, enhancing the power handling capability and the reliability of high power MMICs. We no longer have to resort to fragile, thin chips to satisfy heatsinking requirements.

Coplanar waveguide (CPW) based circuitry, with all components on the same side of a substrate, is used in the flip chip MMICs to facilitate easy ground electrode access on the top surface, eliminating the need for via hole ground connection. Thick silicon dioxide layers are used to support on-chip electrical crossovers , and to provide a protective coating for all circuit elements (Fig. 2),, replacing fragile air-bridges and exposed metalization found on conventional MMICs, both of which are potential reliability problems.

Our focused effort in this new technology development area has led to the demonstration of a robust silicon dioxide coated flip chip MMIC fabrication procedure. A silver plating process has been successfully integrated into the SiO_2 supported bridge fabrication step to form tall (75 mm to 90mm height) bumps for off-chip electrical interconnect. A multi-layer, multi exposure photoresist process was developed to fabricate thermal bumps with a T-shaped cross section (Fig. 3). These T-shaped thermal bumps provide an enlarged foot print at the flip chip/module substrate interface, leading to further reduction of spreading

95CH3577-7/95/0000-0123$01.00 © 1995 IEEE

results shown in Table 2. In addition, the high thermal conductivity of the plated silver bumps serve to equalize the channel temperature of multiple cell, large size transistors on flip chip MMICs (Fig. 4), resulting in the elimination of "hot spots" at the active device areas.

We have established equivalent circuit models for key active and passive circuit elements, including dielectric coated MESFETs (0.3 mm, 1 mm 2 mm and 3.3 mm gate width), coplanar waveguides, spiral inductors and capacitors. The most significant effect of dielectric coating on transistor electrical performance is a two-fold increase in source-drain capacitance. This additional fringe capacitance can be used to our advantage in high efficiency power amplifier design where a low, reactive impedance for all the harmonic frequencies is highly desirable.

The effect of thick (up to 4 mm total) silicon dioxide coating on circuit element rf characteristics, thermal, and reliability test results will be discussed in our presentation. We will also present test data of microwave components designed based on our electronic/thermal circuit element models.

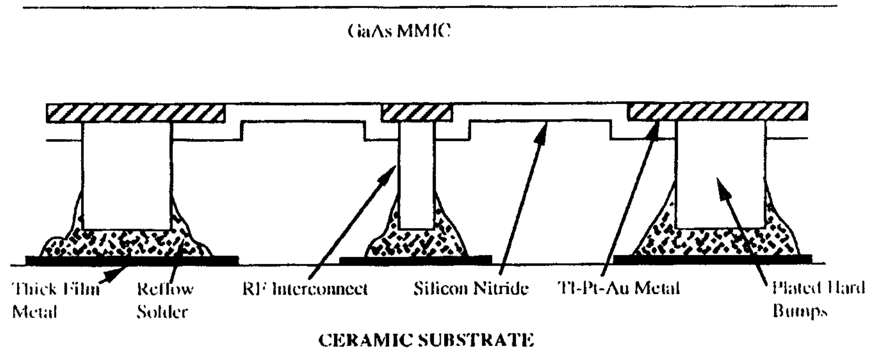
TABLE 1 ADVANTAGES OF DIELECTRIC COATED FLIP-CHIP MMICS

	ADVANTAGE OF FLIP CHIP MMIC T/R MODULE	CONVENTIONAL MICROSTRIP T/R MODULE
MECHANICAL STRENGTH	RUGGED, THICK (625 mm) CHIPS, compatible with proven robotics manufacturing methods, CRITICAL FOR PROCESSING LARGE DIAMETER WAFERS.	Fragile, thin (100 mm) chips, difficult for both chip handling and wafer processing.
RELIABILITY IMPROVEMENT	DIELECTRIC COATED CIRCUITRY WITH MULTI-LAYER METAL INTERCONNECTS, NO AIR-BRIDGE, NO VIA HOLE, NO BACK-SIDE METALIZATION. Proven solder reflow, reliable production module assembly process.	Exposed metal, un-supported air-bridges, via hole ground interconnect, and multiple wire bonds are potential reliability problems.
THERMAL PROPERTY IMPROVEMENT	Improved power handling capability with T-SHAPED PLATED THERMAL BUMPS on active circuit elements.	Fragile, thin chips required to reduce thermal resistance.
T/R MODULE PRODUCIBILITY IMPROVEMENT	PRECISION, SELF-ALIGNED, SINGLE STEP, solder reflow multi-chip module assembly.	Labor intensive sequential multi-chip, multi-wire-bond module assembly.

TABLE 2 PEAK TEMPERATURE RISE OF TRANSISTORS AT 0.70 W/mm POWER DISSIPATION (TRANSISTORS ON ALUMINUM NITRIDE SUBSTRATE)

	3.3 mm FET	1.0 mm FET	0.3 mm FET
Conv face up, (100 mm GaAs)Conv	*95.9°C*	*72.6°C*	*54.0°C*
Conv. face up, (625 mm GaAs)	154.0°C	100.2°C	67.4°C
Flip chip/AIN, (conv. bump)	78.1°C	61.6°C	54.3°C
Flip chip/AIN (T-shape bump)	*68.2°C*	*54.5°C*	*49.0°C*

Fig.1 Flip-Chip Attachment With Solder Reflow Process (Top) and in Final Position (Bottom)



- Low cost, high volume (robotic, self-aligning)
- High yield (solder-bumps)
- Better reliability (no wire bonding)
- 1-step solder reflow process for multi-chip module assembly

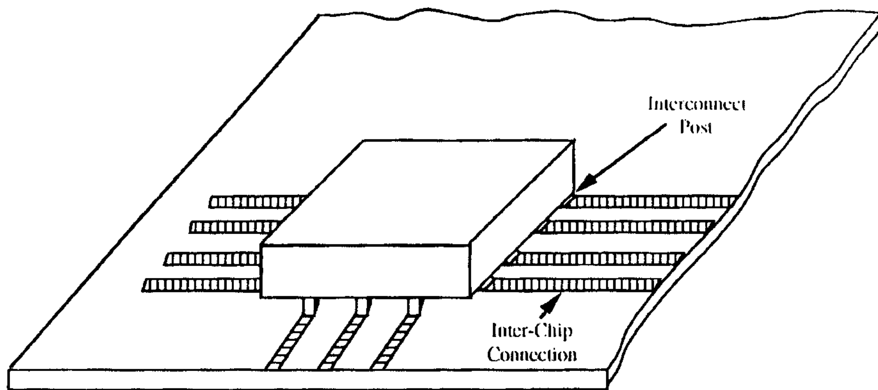


Fig. 2 Dielectric Coated Flip Chip MMIC

* Elimination of air-bridge interconnect
* Elimination of exposed metalization
* Elimination of via hole grounding

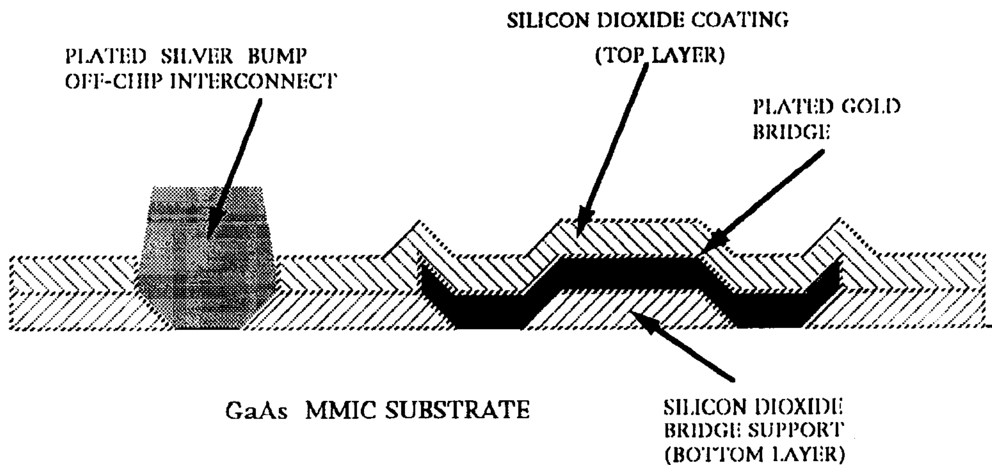


Fig. 3 T-Shaped Plated Silver Thermal Bump
* Enlarged foot print at the flip chip/ module interface reduces spreading thermal resistance

Fig. 4 Thermal Distribution Of A 3.3 mm Flip-Mounted Transistor With A T-Shaped, Plated Thermal Bump (0.7 W/mm Dissipation)